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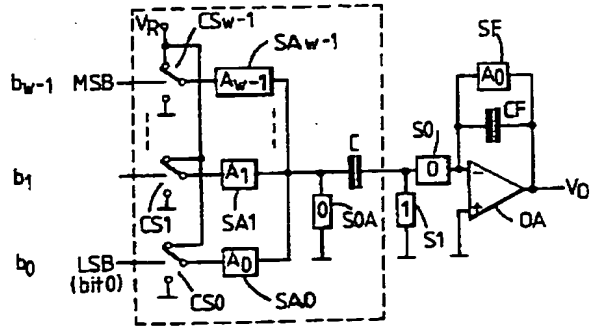
(54) Digital-to-analogue conversion.

(57) A switched capacitor digital-to-analogue converter employing a single capacitor C, common to a plurality of bits b,b_{w-1}, appropriate weighting of the bits being achieved by switching waveforms A_0 to A_{w-1}.

Fig.6.



EP 0 604 397 A2

This application is a divisional application of European Patent Application No. EP-A-344998 and relates to digital-to-analogue converters and their use in filtering arrangements.

A typical, conventional filtering arrangement is shown in Figure 1, where successive sample values of a w-bit digital word $[b_0 b_1 ... b_i ... b_{w-1}]$ are supplied to a digital-to-analogue converter (DAC) 1 followed by an analogue FIR (finite impulse response) filter 2, based on a conventional tapped delay line structure with delays z^{-1}, filter coefficient multipliers $h_0 ... h_{N-1}$ and an adder A (or of course a parallel structure may be used). The coefficients are selected to give any desired filter response; in general this will be a baseband response from DC to half the sampling frequency F_S, followed by some rejection of unwanted frequencies above $F_S/2$.

The DAC may employ switched capacitor techniques (as described for example in Roubik Gregorian - "High Resolution Switched Capacitor D/A Converter" - Microelectronics Journal, Vol. 12, No. 2, 1981 Mackintosh Publ. Ltd); in the filter, the analogue delays may also be realised by switched-capacitor elements. The realisation of the analogue delays may however not be ideal.

Alternatively, the delays may be achieved digitally as described in US Patent No. 3,543,009 (Voelcker). An arrangement using this principle shown in Figure 2 and receives, as does that of Figure 1, successive w-bit digital samples of a signal to be converted. The digital words are fed to a chain of N w-bit wide D-type bistable flip-flops DO...DN-1 which are clocked at sampling rate F_S with clock pulses Ø, so that a digital word, delayed by a respective number of sample periods, is available at the output of each flip-flop. These outputs are converted into analogue form by digital-to-analogue converters XO...XW-1 which produce at their outputs successive analogue samples corresponding to the digital samples supplied to them. The analogue outputs are multiplied by respective filter coefficients $h_0 ... h_{N-1}$; multipliers MO...MN-1 are shown though in the US patent resistors are used. The weighted analogue values are then summed in an adder A.

According to one aspect of the present invention there is provided a switched capacitor digital-to-analogue converter comprising inputs for receiving signals representing respective bits of a digital signal, respective switching means for supplying charge to a capacitor in dependence on the states of those bits, and means for generating an analogue output signal representing the sum of those charges, characterised in that the said capacitor is a single capacitor common to all bits and that the switching means are arranged to supply, in response to each of said inputs, a respective switching waveform, each waveform comprising a different predetermined number of pulses, said number corresponding to the significance of the respective bit such that the charges supplied are weighted according to the significance of the bits.

Preferably the digital signal comprises w bits and the switching waveforms comprise 2^i pulses, where i is an integer from 0 to w.

The digital-to-analogue converter maybe used in a filter apparatus, as described in the parent application. The desired filter response may be achieved by choosing the values of the capacitor in one (or more) switched-capacitor arrangements to have a value different from the corresponding capacitor in another.

Some embodiments of the present invention will now be described, by way of example, with reference to the accompanying drawings, in which: -

- Figure 3 is a circuit diagram of a known switched-capacitor unit;
- Figure 3a illustrates clock pulses used by the unit of Figure 3;
- Figure 4 is a block diagram of a further embodiment of filtered digital-to-analogue converter;
- Figure 5 is a modified version of part of Figure 3, for implementing negative filter coefficients;
- Figure 6 is a circuit diagram of a digital-to-analogue converter unit;
  Figure 7 illustrates the clock and switching pulses employed in the unit of Figure 6;
- Figure 8 is a block diagram of a filtered digital-to-analogue converter employing converter units of the type shown in Figure 6;
- Figure 9 is a modified version of part of Figure 6, for implementing negative filter coefficients;
- Figure 10 illustrates a practical implementation of the converter of Figure 8;
- Figure 11 is a block diagram of a pulse generator for driving the converter of Figure 10; and
- Figure 12 is a state diagram illustrating the operation of the generator of Figure 10.

First, the operation of a known type of switched capacitor digital-to-analogue converter will be described with reference to Figure 3, where the input bits of a w-bit digital word are designated $b_0 ... b_{w-1}$ and each serves to switch, according to its binary value, an electronic switch CSO...CSw-1 (shown schematically) between zero volts (referred to below as "ground") and a reference voltage V_R.The converter contains a number of electronic switches controlled by the non-overlapping two-phase clock pulses $Ø_0$, $Ø_1$ at the sampling frequency F_S, which are shown in Figure 3a. In Figure 3 and elsewhere, the switches are shown as rectangles containing 0 or 1 indicating that the switch is closed during clock phase 0 or 1 respectively. Using the suffix i to indicate generically the components handling signals from one bit (b_i) of the input bits

$b_0 \ldots b_{w-1}$, the output of each switch CSi is connected via a switch s1i controlled by $\emptyset_1$ to one side of a capacitor CPi, which is also connected to ground via a switch SOi controlled by $\emptyset_0$. The other side of each capacitor CPi is connected to a common node ND, also connected to ground by a switch S1 controlled by $\emptyset_1$. The capacitors have binary weighted values - i.e. the capacitance of the capacitor CPi is 2^i.C where C is the value of the smallest capacitor CP0. The node ND is also connected via a switch SO controlled by $\emptyset_0$ to the input of a high gain inverting amplifier OA which has a negative feedback path consisting of a capacitor C_F in parallel with a switch S1F controlled by $\emptyset_1$.

During clock phase 1, the capacitor C_F is discharged via S1F. Also, each capacitor CPi is charged or discharged via switches S1i and S1 to the voltage (0 or V_R) determined by the respective switch CSi. During clock phase ϕ_0, the total charge on the capacitors CPi

$$Q = \sum_{0}^{w-1} b_i . V_R . 2^i . C = CV_R \sum_{0}^{w-1} b_i 2^i$$

is transferred to the capacitor C_F so that the output of the converter is

$$V_0 = \frac{C V_R}{C_F} \sum_{i=0}^{w-1} b_i 2^i \qquad \ldots (1)$$

Figure 4 shows a filtered digital-to-analogue conversion apparatus according to a first embodiment of the invention where the node ND, switches S0, S1, S1F, capacitor C_F and amplifier OA are common to the N converters. The flip-flops DO...DN-1 are as in Figure 2, whilst the capacitor/switch array units CSAO...CSAN-1 correspond to the components enclosed in the broken line box in Figure 3. In this embodiment, the capacitor values in each array are chosen to weight the contribution of that array to the final output by a factor corresponding to the appropriate one of the desired filter coefficients $h_0 \ldots h_{N-1}$.

To accommodate negative coefficients, the array is modified by the transposition of the clock phases illustrated in Figure 5 by transposition of switches S0i and S1i. The nth array (n = 0,....,N-1) has capacitors with values $2^i.C_n$ where $C_n = |h_n|.C^*$ (C^* being a constant), so that the contribution of this array to the total output voltage is

$$V_{o,n}(z) = h_n \frac{C^*}{C_F} V_R \left(\sum_{i=0}^{w-1} b_{i,n} . 2^i\right) z^{-n} \qquad \ldots (2)$$

where z is the z-transform variable and $b_{i,n}$ is the value of the ith bit of the digital word at the output of the nth D-type flip-flop. The contribution of all N words for a FIR filter of length N is

$$V_o(z) = \sum_{n=0}^{N-1} V_{o,n}(z)$$

$$V_o(z) = \frac{V_R}{C_F} \sum_{n=0}^{N-1} \left[h_n . C^* \left(\sum_{i=0}^{w-1} b_{i,n} 2^i\right) . z^{-n}\right]$$

If we set $C_F = 2^w.C^*$ then the output voltage is

$$V_o(z) = V_R \sum_{n=0}^{N-1} h_n . \left(\sum_{i=0}^{w-1} b_{i,n} . 2^{i-w} \right) . z^{-n}$$

If the smallest capacitance value C_n is C, and the corresponding value of h_n is $h_{n\ min}$ then the remaining capacitor values are given by

$$C_n = \frac{|h_n| . C}{|h_n|_{min}}$$

and

$$C_F = \frac{2^w . C}{|h_n|_{min}}$$

Since C_F is usually the largest capacitor in the circuit, we obtain a maximum capacitance spread of

$$\frac{C_F}{C_{n\ min}} = \frac{2^w}{|h_{n\ min}|}$$

and a total capacitor area of

$$C_{total} = \frac{C}{|h_n|_{min}} \left[2^w + (2^w - 1) . \sum_{n=0}^{N-1} |h_n| \right]$$

For an example of FIR filtering function with equal coefficients and unity DC gain ($h_n = 1/N$, n = 0, ..., N-1) the above results lead to a capacitance spread of $C_{spread} = N.2^w$ and a total capacitor area of

$C_{total} = N.(2^{w+1}-1).C.$

The embodiment of Figure 4 requires (N.w) + 1 capacitors and (2N.w) + 3 switches, increasing with both the bit resolution w of the conversion and the length N of the desired filter impulse response. This means that, even for a medium bit resolution and short filter responses, the resulting silicon area required for an integrated circuit implementation can become rather large. An alternative converter is however now proposed, having reduced number of capacitors and switches.

Figure 6 shows a switched capacitor digital-to-analogue converter (without filtering). It can, as will be described in more detail below, be used to replace the converters X0..XN-1 of Figure 2, in the same manner as was the converter of Figure 3.

Input bits b_i and switches CSi perform the same functions as in Figure 3, as do switches S1, S0, SF, capacitor C_F and amplifier OA. However, the capacitors CPi and switches $S0_i$ are replaced by a single capacitor CP and switch S0A. The binary weighting of contribution of the w input bits is instead determined by the waveforms applied to the switches S1i (now designated SA0....SAi...SAw-1). Effectively the capacitor CP is multiplexed between the input bits. A set of switching waveforms ϕ'_1, ϕ'_0 and $A_0..A_{w-1}$ for w = 3 is

illustrated in Figure 7.

Note that there are now 2^{w-1} clock pulses ϕ_1' (or ϕ_0') in one conversion period. The waveforms $A_0 ... A_{w-1}$ contain 1, 2, 4 etc pulses synchronous with ϕ_1' - ie in general the waveform A_i contains 2^i pulses. At the beginning of each conversion period, the feedback capacitor C_F is reset by the switch SF controlled by pulse A_0. Pulse A_0 also closes switch SAO and the capacitor C assumes a voltage of 0 or V_R according to the state of bit b_0. On the following clock pulse ϕ_0' this charge is transferred to C_F. This process is repeated by pulse A_1 for bit b_1; however, this occurs twice, as A_1 contains two pulses, and so forth, the D/A conversion being performed sequentially from bit b_0 to bit b_{w-1}. The converted output is available during pulse ϕ_0 following the last pulse of A_{w-1}, prior to resetting of C_F by a further pulse A_0. Of course it is not actually necessary that the bits be processed in any particular sequence, or indeed that all the pulses for one particular bit be generated before those of another bit (though obviously the pulses must not coincide).

The equivalent bit voltage V_i corresponding to each bit of the digital word is determined by the number of pulses of the corresponding switching waveform A_i and can thus be expressed by

$$V_i = V_R.b_i.2^i$$

and therefore the converted output is

$$V_o = \frac{C\,V_R}{C_F} \sum_{i=0}^{W-1} b_i . 2^i$$

Assuming $[V_0 \text{ max } /V_R.(1-2^{-N})] = 1$, we can easily see from the above expression that the capacitance spread of the converter in Figure 6 is equal to the capacitance spread of the conventional converter of Figure 3, ie $(C_F/C) = 2^w$. However, the total capacitor area is now only $(2^w + 1).C$, compared to $2^{w+1}.C$ in a conventional converter, and the total number of capacitors has also been reduced from $(w + 1)$ to only 2. An additional significant advantage of this new architecture is that, unlike conventional converters, the accuracy of the capacitance ratio C_F/C does not affect the required bit resolution, which depends solely on the number of time slots of each switching waveform. Thus, we can easily apply to the converter of Figure 6 a number of well known design techniques than can significantly reduce the capacitance spread in a switched-capacitor network (eg capacitive-T network), even though this also brings an inherent reduction of the resulting accuracy of the capacitance ratios. This makes it practical to implement high resolution converters using simple switched capacitor networks occupying a small area of silicon.

It is observed that, for a given maximum switching frequency, the conversion rate (and hence sampling rate of the digital words that can be accommodated) is reduced by a factor of (2^w-1) relative to Figure 3; however the reduction in capacitor area and required capacitance ratio accuracy make this embodiment particularly useful for high resolution conversions at lower frequency.

An implementation of a combined digital-to-analogue converter and FIR filter based on the binary-weighted time slot array architecture described above is illustrated in Figure 8. The flip-flops Dn are shown as for Figures 2 and 4. The converters Xn of Figure 2 are replaced by time slot arrays TA0 to TAN-1, followed by common components S1, S0, OA, C_F and SF which are identical to those shown in Figure 6. Each time slot array TAi is either in the form indicated in the dotted rectangle in Figure 6 (for positive h_n) or, for negative h_n is structurally the same but is supplied with different pulses. Thus switches SAn supplied by pulses A_n and switch SOA supplied with pulses ϕ_0' are replaced by switches SBn and S1A supplied with pulses B_n and ϕ_1', as shown in Figure 9. Pulses B_n $(n = 0...n-1)$ take the same form as pulses A_n but are synchronous with ϕ_0' instead of ϕ_1'.

As in the case of the architecture of Figure 2, we can easily see that the normalised output voltage conversion level corresponding to all N digital words is also expressed by

$$\frac{Vo(z)}{V_R(1-2^{-N})} = \frac{1}{C_F} \sum_{n=0}^{N-1} [C_n . (\sum_{i=0}^{W-1} b_{i,n} 2^i) . z^{-n}]$$

where

$$C_n = \frac{|h_n| \cdot C_F}{2^W}$$

in order to preserve the gain constant of the FIR transfer function. After normalisation, we obtain

$C_{n\,min} = C$

$$C_n = \frac{|h_n| \cdot C}{|h_{n\,min}|}$$

$$C_F = \frac{2^W \cdot C}{|h_{n\,min}|}$$

yielding a maximum capacitance spread of

$$C_{spread} = C_F / C = \frac{2^W}{|h_{n\,min}|}$$

and

$$C_{total} = \frac{C}{|h_{n\,min}|} \left(2^w + \sum_{n=0}^{N-1} h_n\right)$$

for the total capacitor area. For many practical situations where the FIR filter is designed such that

$$\sum_{n=0}^{N-1} h_n = 1$$

the above expression for C_{total} shows a reduction of about 50% over the total capacitor area obtained with the previous realisation. Two additional advantages of the architecture with binary-weighted time slot arrays are obtained firstly with respect to the total number of capacitors, which has been reduced from (N.w + 1) to only (N + 1), and, secondly, with respect to the required capacitance ratio accuracy of the impulse response coefficients of the FIR filter.

Figures 10 and 11 illustrate a simple practical implementation of the type of combined digital-to-analogue converter described above with reference to figure 8. It has 4-bit resolution and four equal FIR filter coefficients. The filter impulse response (in z-transform notation) is

$H(z) = 1/4\,(1 + z^{-1} + z^{-2} + z^{-3})$.

There are four 4-bit wide D-type flip-flops D0, D1, D2, D3. Note that the first of these is (as in the other figures) not strictly necessary but is included to ensure accurate timing. Also the switches CSi are omitted (on the basis that, for a 4-bit implementation, the voltages output directly from the flip-flops are themselves sufficiently consistent). There are three stages TAN0 ... TAN3, of the type shown in figure 6, with equal capacitor C0 ... C3 (= capacitance C) representing the four equal coefficients. Components S0, S1, SF, CF

and OA are as shown in figure 6, whilst two simple sample and hold circuits SW1, CH1, OA1, SW2, CH2, OA2 are included to sample the output (A_0 being applied to switches SW1, SW2) when conversion is completed, to eliminate any output transients during conversion. C_F is equal to 64C for V_{omax}/V_R $(1 - 2^{-N})$ = 1.

The switching waveforms A_0, A_1, A_2, A_3 are generated by means of the generator shown in figure 11. A square-wave oscillator OSC drives a non-overlapping phasing generator consisting of an invertor I1, cross-coupled NAND gates N1, N2, and inverters I2, I3 to produce pulses ϕ_0, ϕ_1. A modulo 8 binary down-counter Z is clocked by ϕ_1. The ' 1111' state is designated as an idle-state in which the counter is locked by an and-gate AND1 which decodes this state to an end of conversion pulse EOC and inhibits clock pulses via a switch SWI in the oscillation circuit.

The generation of the required (2^w-1) = 15 pulses of the switching waveforms A_0 ... A_3 is indicated by an external pulse SOC (synchronous with the digital input data to be converted) which is applied to a paralled load input PE of the counter Z1 to load count ' 1110' into the counter.

The counter is then decremented by pulses ϕ_1 through its states to 000, during which period the counter states are decoded by inverters I4 ... I7 and and-gates AND2 ... AND4 to produce the pulses A_0 ... A_3 as illustrated in the sequence diagram in figure 12. The sixteenth pulse ϕ_1 returns the counter to the ' 1111' state where it remains locked until a further start pulse SOC is received.

Note that in this converter, pulses B_i are not required (since the filter coefficients are all positive) but could of course be generated by a second counter and decoding logic similar to the arrangements for A_i.

A discrete component version of this converter can be constructed using amplifiers type LF353, CMOS analogue switches type CD4016, and standard CMOS logic circuits, although in practice an integrated circuit implementation is to be preferred.

Typical capacitor values are C = 40pF and C_F = 2700pF (with ± 0.2% of the nominal values) may be used.

Claims

1. A switched capacitor digital-to-analogue converter comprising inputs for receiving signals representing respective bits of a digital signal, respective switching means (CS1...CSw-1, SA0...SAw-1) for supplying charge to a capacitor in dependence on the states of those bits, and means for generating an analogue output signal representing the sum of those charges, characterised in that the said capacitor is a single capacitor (C) common to all bits and that the switching means (CSi, SAi) are arranged to supply, in response to each of said inputs, a respective switching waveform (A_0 to A_{w-1}), each waveform comprising a different predetermined number of pulses, said number corresponding to the significance of the respective bit such that the charges supplied are weighted according to the significance of the bits.

2. A digital-to-analogue converter according to Claim 1 wherein the digital signal comprises w bits and the switching waveforms comprise 2^i pulses, where i is an integer from 0 to w.

3. A digital-to-analogue converter according to Claim 1 or 2 wherein the switching waveforms are supplied sequentially for each bit of the digital signal.

4. An apparatus for producing a filtered analogue output signal from a digital signal in the form of a sequence of digital signal samples each having a plurality of bits comprising digital delay means (D0...DN-1) for producing further sequences of digital signal samples, each being a replica of the first sequence delayed with respect thereto by a respective delay period, a plurality of switched capacitor digital-to-analogue converters as claimed in any of claims 1 to 3, each connected to receive a respective one of the said sequences of digital signal samples and the total charge of each switched capacitor digital-to-analogue converter being weighted to weight the contribution of each converter by a factor corresponding to a respective one of a set of coefficients corresponding to a desired filter response, and common summing means (S0, S1, SIF or SF, CF, OA) for receiving the charges from all the switched capacitor digital-to-analogue converters and forming an analogue output sequence representing the sum of those charges.

5. An apparatus according to Claim 6, characterised in that the capacitor in at least one of the switched capacitor digital-to-analogue converters differs in value from the corresponding capacitor in another of the switched capacitor digital-to-analogue converters, such as to weight the charges by factors

corresponding to the said coefficients.

Fig.1.
PRIOR ART

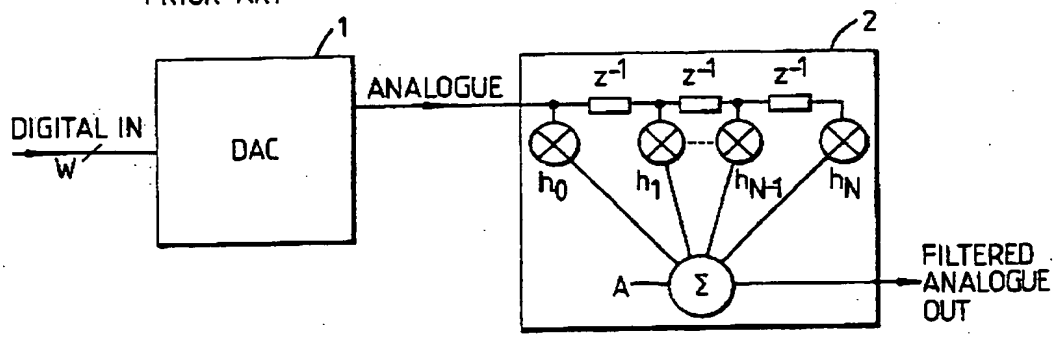
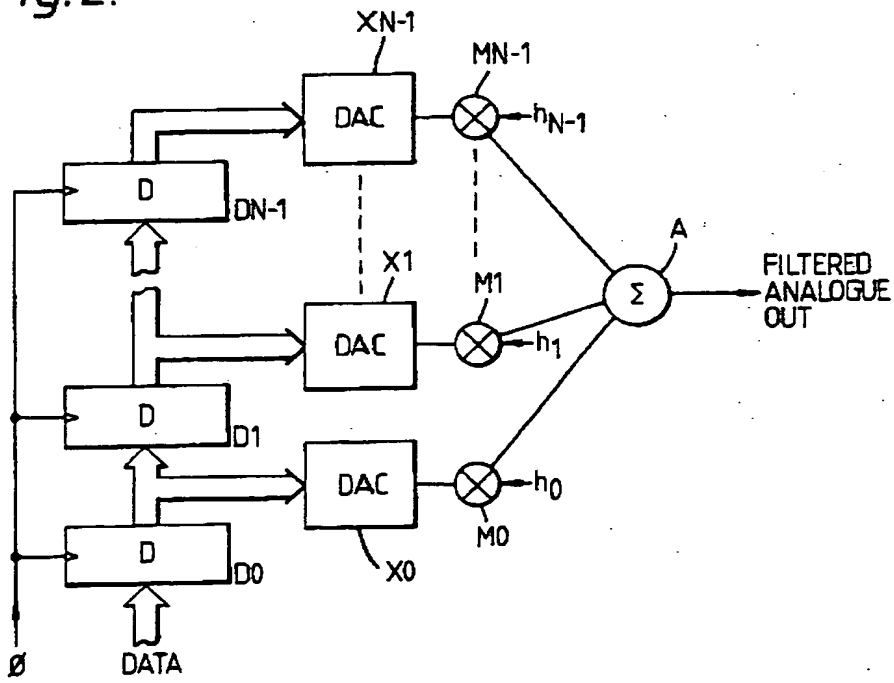


Fig.2.



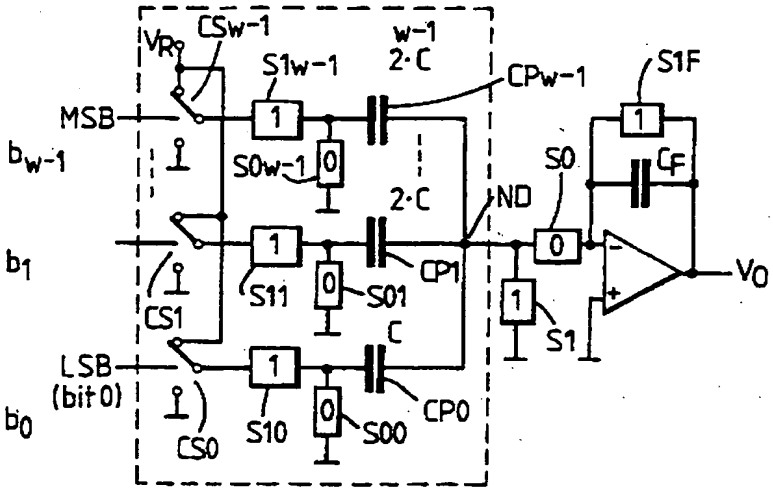


Fig. 3.
(PRIOR ART)

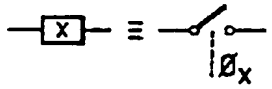


Fig. 3a

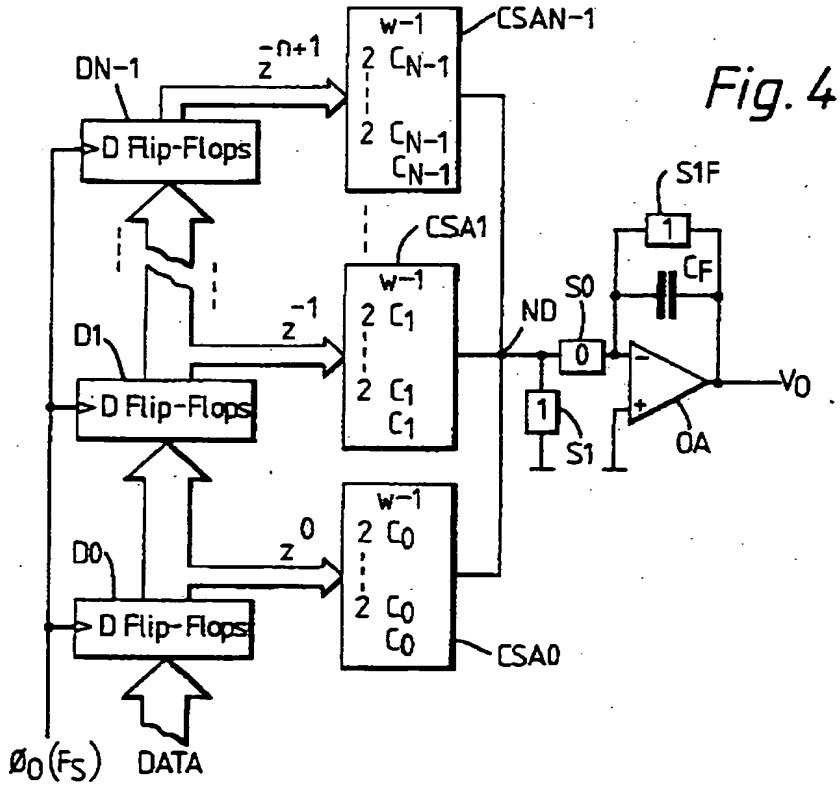
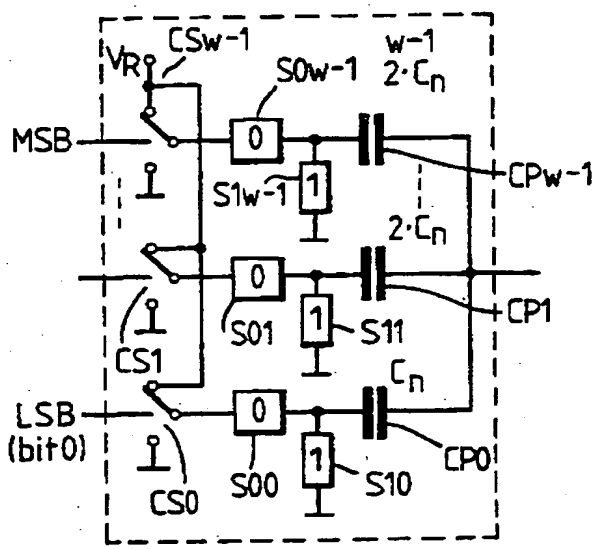


Fig. 4.

Fig.5.



CAPACITOR ARRAY AND SWITCH ARRANGEMENT FOR $h_n<0$

Fig.6.

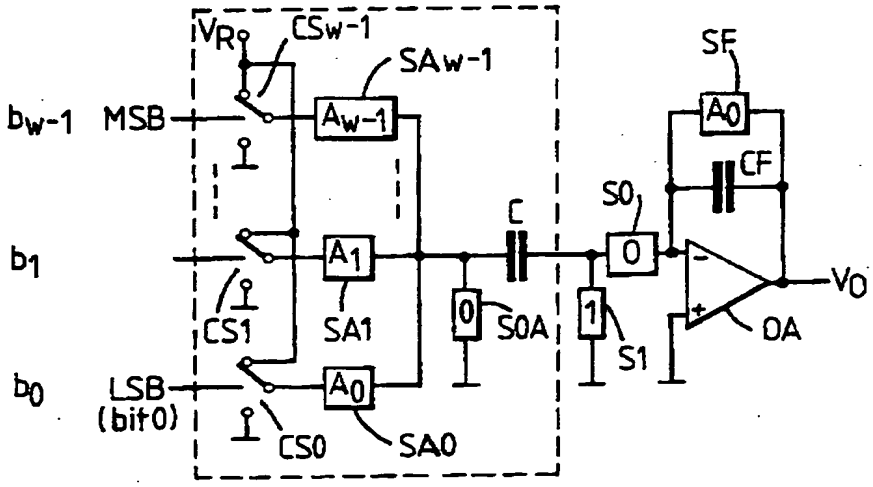


Fig. 7

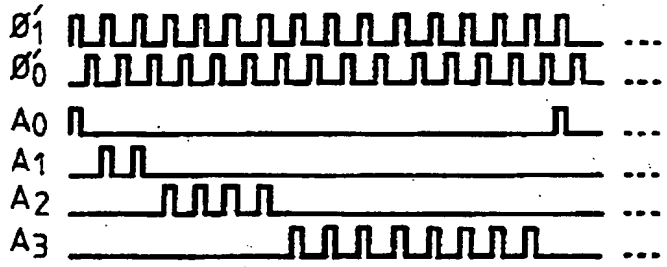

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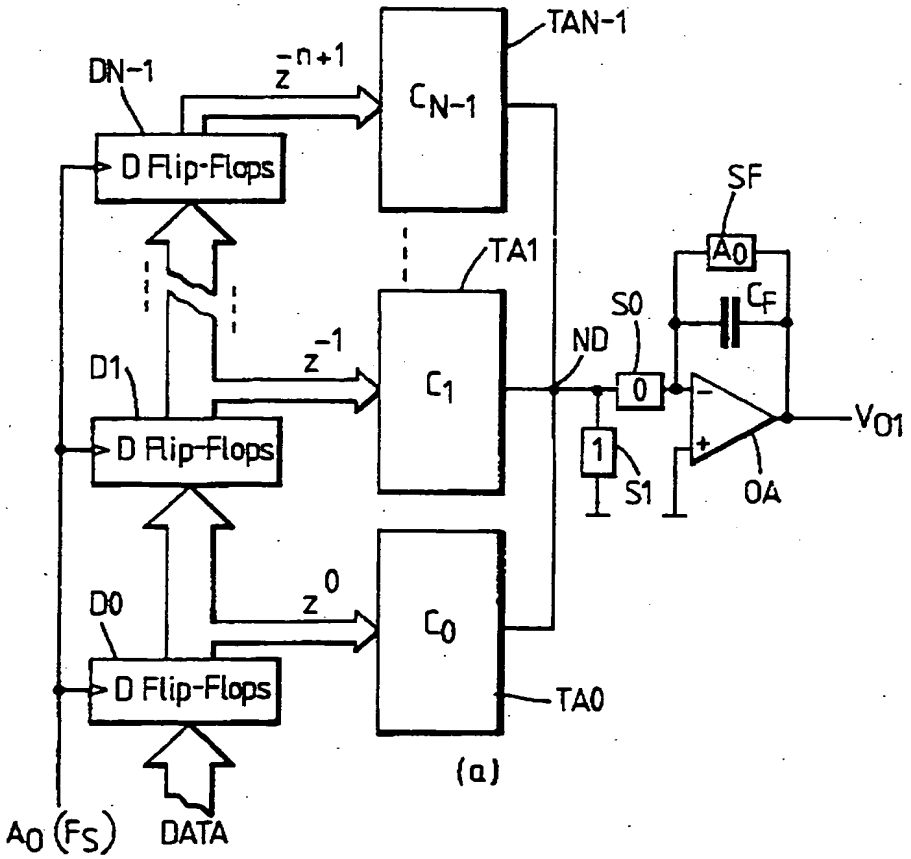
Fig. 8.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A_0 (Fs)
DATA

Fig. 9.

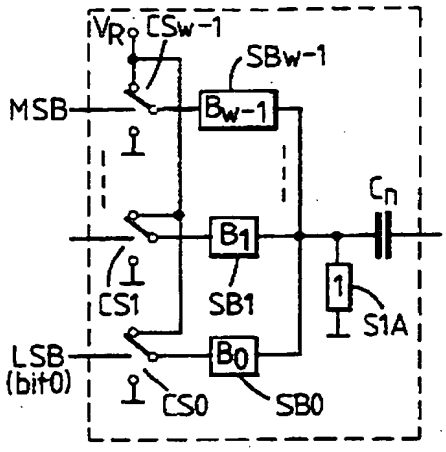
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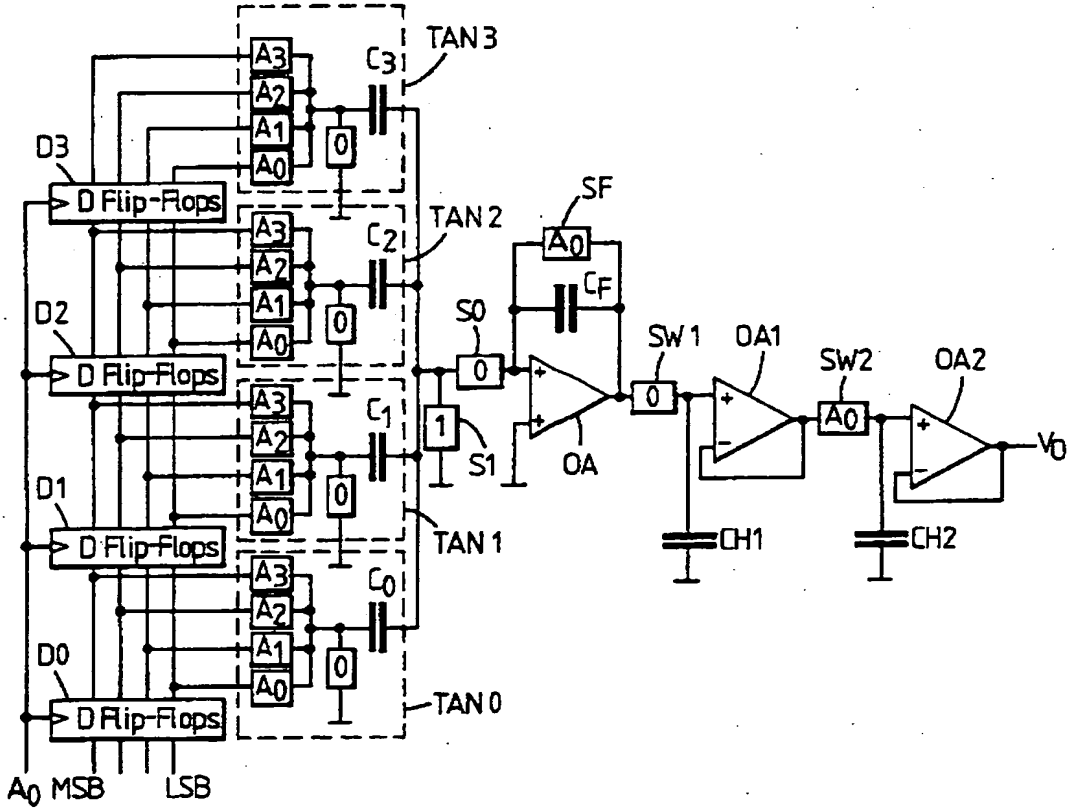
Fig.10.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C0
D0
TAN0
A0 MSB
LSB

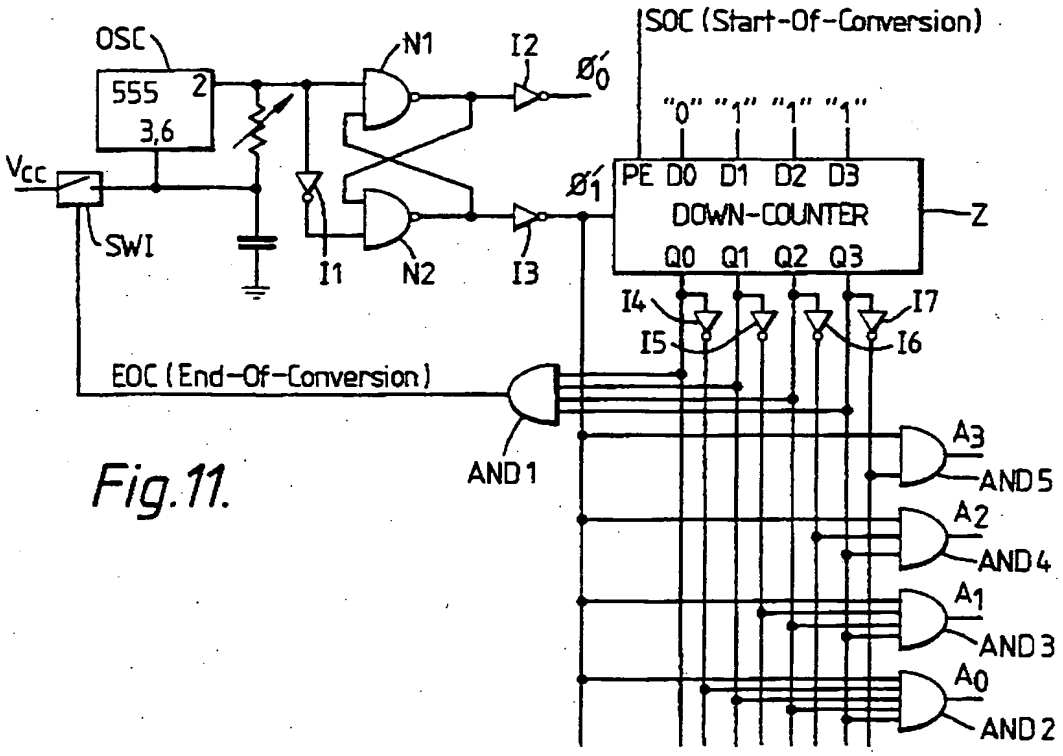
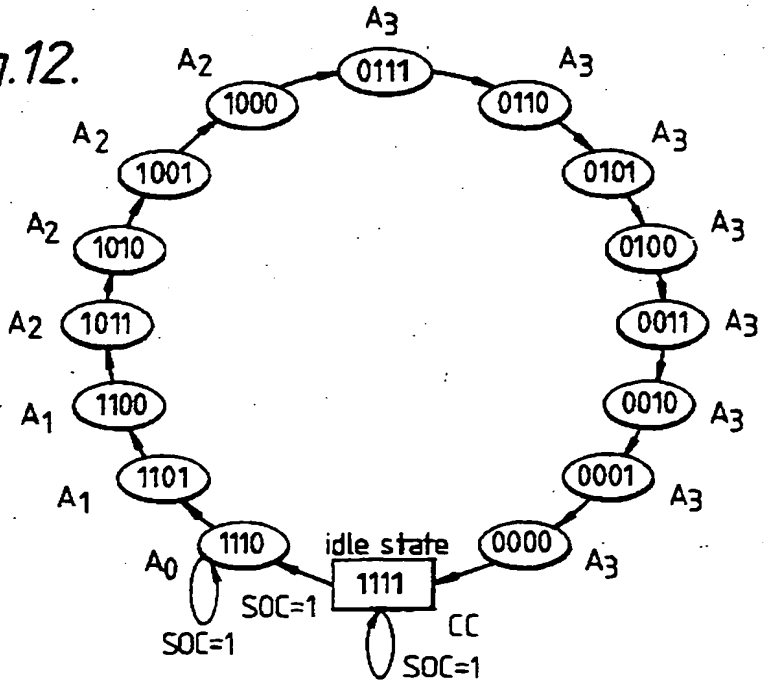

OSC
555
3,6
2
Vcc
SWI
N1
I2
Ø'0
Ø'1
I1
N2
I3
SOC (Start-Of-Conversion)
"0" "1" "1" "1"
PE D0 D1 D2 D3
DOWN-COUNTER
Z
Q0 Q1 Q2 Q3
I4
I5
I7
I6
EOC (End-Of-Conversion)
AND1
A3
AND5
A2
AND4
A1
AND3
A0
AND2

Fig.11.

Fig.12.


A3
0111
A2
1000
A3
0110
A2
1001
A3
0101
A2
1010
A3
0100
A2
1011
A3
0011
A1
1100
A3
0010
A1
1101
A3
0001
A1
1110
idle state
0000
A3
A0
1111
SOC=1
CC
SOC=1
SOC=1